Reference Clock Frequency 1000 M/ $_{\rm Z}$ Example synthesis of 734.3133739 M/ $_{\rm Z}$ , with 12 bit math/delay Increment value = (  $2^{i2}$ . \*1000MHz/734.3133739MHz) - $2^{i2}$ 

TABLE 1

Increment Value = 1482

Falling Edge Accumulator Start Value =  $(50\% \text{ of } (1000\text{MHz}/734.3133739\text{MHz})^* 2^{i2}) = 2789$ 

Rising Edge						
Accumulator	Overflow bits	Base Accumulator	Equilvalent Delay from Nearest Ref Edge (deg)	Total Effective Delay (deg)		
0	0	0	0	0		
1482		1482		490.25		
2964	0	2964	260.51	980.51		
4446		350		1470.76		
1832		1832		1961.02		
3314		3314		2451.27		
4796		700				
2182		2182				
3664		3664		3922.03		
5146		1050		4412.29		
2532		2532	222.54	4902.54		
4014		4014		5392.79		
5496		1400				
2882	r .	2882	253.3	6373.3		
4364	1	268	23,55	6863.55		
1750		1750	153.81	7353.81		
3232	Ö	3232	284.06	7844.06		
4714	1	618	54.32	8334.32		
2100	0	2100	184.57	8824.57		
3582	0	3582	314.82	9314.82		
5064	1	968	85.08	9805.08		
2450	0	2450	215.33	10295.33		
3932	0	3932	345.59	10785.59		
5414	1	1318	115.84	11275.84		
2800	0	2800	246.09	11766.09		
4282	1	186	16.35	12256.35		
1668	0	1668	146.6	12746.6		

Falling Edge						
Accumulator	Overflow bits	Base Accumulator	Equilvalent Delay from Nearest Ref Edge (deg)	Total Effective Delay (deg)		
2789	0	2789	245.13	245.13		
4271	1	175	15.38	735.38		
1657	0	1657	145.63	1225.63		
3139		3139	275.89			
4621	1	525	46.14			
2007		2007	176.4			
3489		3489	306.65			
4971	1	875	76.9	3676.9		
2357	0	2357	207.16			
3839	0	3839	337.41	4657.41		
5321	1	1225	107.67			
2707		2707	237,92			
4189		93	8.17	6128,17		
1575		1575	138.43			
3057		3057	268.68			
4539		443	38.94			
1925	0	1925	169.19	8089.19		
3407	0	3407	299.44	8579.44		
4889	1	793	69.7	_		
2275		2275	199.95			
3757		3757	330.21			
5239		1143	100,46			
2625		2625	230.71	11030.71		
4107	1	11	0.97			
1493	0	1493	131.22			
2975	0	2975	261.47	12501.47		
4457	1	361	31.73	12991.73		